Hall Ticket Number:

Code No. : 15404 S

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

B.E. (ECE:CBCS) V-Semester Supplementary Examinations, May/June-2019

Subject: COMPUTER ORGANIZATION AND ARCHITECTURE

Time: **3** hours Max. Marks: **70**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

1. Represent Decimal (-42) in 2's complement form.
2. Compare Fixed and Floating point data representations
3. List the characteristics of RISC core.
4. Define stored program organization and its necessity in basic processor architecture.
5. Neatly sketch the Block diagram of Associative memory.
6. Define page fault? List the page replacement algorithms.
7. Define Memory segmentation in 8086μp? List the advantages of it.
8. With a neat timing diagram explain memory READ operation in minimum mode operation of 8086μp?
9. Explain the register format of CWR of 8255 PPI?
10. What is the necessity for DMA in a computer system?

Part-B (5 × 10 = 50 Marks)

11. a) Explain the restoring method of fixed point binary division with a neat Flowchart. [5]
    b) Calculate (11/3) using above method, Showing the step by step procedure. [5]

12. a) Define an Addressing mode. Explain one address, two address and three address instruction formats and Give an example for each. [5]
    b) Explain the operation of instruction pipeline with a neat diagram? [5]

13. a) Signify the importance of Memory Hierarchy in a computer organization, and represent the Hierarchy with a neat diagram. [5]
    b) Explain the concept of virtual memory and represent the process of mapping page address? [5]

14. a) Distinguish between Minimum and Maximum modes of operations of 8086μp with help of block diagrams. [6]
    b) Write an assembly language program to find out the maximum number from any list of five signed numbers. [4]

15. a) Explain the operation of 8255 PPI with a neat block diagram? [5]
    b) Explain the architecture of 8251 USART. [5]

16. a) Write a short note on Evolution of computer generations. [5]
    b) Explain the operation of microprogram sequencer? [5]

17. Answer any ***two*** of the following:
    a) Explain about daisy chaining priority based interrupt method with a neat diagram? [5]
    b) Write a brief note on stack operation of 8086μp and signify it's importance in calling an interrupt subroutine? [5]
    c) Show interface diagram of 2 chips of 4KX8 Memory ICs with 8086μp? [5]

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